

Faculty Profile

Faculty Name	Sandeep Kumar
Designation	Assistant Professor (ECE)
Qualification	Ph.D.*, UGC-NET, M.Tech. (VLSI Design), M.Sc. (Electronics Science), B.Sc. (Electronics)
Email	vlsi.sandeep@gmail.com
Area of Interest	Design and Modeling of Multigate Semiconductor Devices
Work Experience (Total)	12 years
<ul style="list-style-type: none"> • Teaching 	9.5 years
<ul style="list-style-type: none"> • Research 	2.5 years
<ul style="list-style-type: none"> • Industry 	
<ul style="list-style-type: none"> • Others 	
Courses taught at Diploma/ Post Diploma/ Under Graduate/ Post Graduate/ Post Graduate Diploma Level	VLSI Design, Digital VLSI Design, VHDL, Digital VLSI Design using Verilog, Digital Electronics
Membership of Professional Bodies	
Research Publications	01
<ul style="list-style-type: none"> • Research Papers UGC-CARE 	
<ul style="list-style-type: none"> • Research Papers SCOPUS 	
<ul style="list-style-type: none"> • Research Papers WoS/SCI/ABDC 	01
<ul style="list-style-type: none"> • List of Publications 	Sandeep Kumar, Arun Kumar Chatterjee and Rishikesh Pandey, "Performance Analysis of Gate Electrode Work Function Variations in Double-gate Junctionless FET, Silicon, 2020.
Book and Chapter Publications	
<ul style="list-style-type: none"> • Books Authored published by International Publishers 	
<ul style="list-style-type: none"> • Books Authored published by National Publishers 	
<ul style="list-style-type: none"> • Publication of Chapter in Edited Books 	
<ul style="list-style-type: none"> • Editor of Book by International Publishers 	
<ul style="list-style-type: none"> • Editor of Book by National Publishers 	
<ul style="list-style-type: none"> • Translation Work of Book 	
<ul style="list-style-type: none"> • List of Book and Chapter Publications 	
Patents	

<ul style="list-style-type: none"> • Published 	
<ul style="list-style-type: none"> • List of published patent(s) 	
<ul style="list-style-type: none"> • Filed 	
<ul style="list-style-type: none"> • List of filed patent(s) 	
PhD Guidance	
<ul style="list-style-type: none"> • Degree Awarded 	
<ul style="list-style-type: none"> • Thesis Submitted 	
M.Tech. Guidance	
<ul style="list-style-type: none"> • Degree Awarded 	
<ul style="list-style-type: none"> • Thesis Submitted 	
Research Project	
<ul style="list-style-type: none"> • List of Research project 	
Consultancy	
<ul style="list-style-type: none"> • List of Consultancy 	
Awards & Honours	
<ul style="list-style-type: none"> • List of Awards & Honours 	
Invited lectures / Resource Person/ paper presentation in Seminars/ Conferences/full paper in Conference	
<ul style="list-style-type: none"> • International (Abroad) 	02
<ul style="list-style-type: none"> • International (Within Country) 	01
<ul style="list-style-type: none"> • National 	03
<ul style="list-style-type: none"> • List of published papers 	<ol style="list-style-type: none"> 1. Sandeep Kumar, K.K. Paliwal and Sudhir Mahajan, "Effect of reduction in Gate Oxide Thickness with different materials for 100 nm MOSFET", IJLRST, Volume 7, Issue 1, pp. 58, ISSN (Online): 2278-5299, February 2018,. 2. Ritu Munjal, Sandeep Kumar, "Hardware Implementation of Neural Network based Fault Classifier System of CRO", International Journal of Computational Engineering & Management, Volume 16, Issue 3, May 2013. [IC Value 4.14]. 3. B. Singh, Sandeep Kumar, Sunil Kumar and K. Sheoran, "Embedded Systems/RTOS: An Overview, ETECE, PIET, Samalakha, April 2013. 4. Sandeep Kumar, Ritu Munjal, B. Singh and Anita Jain, "3D Integration with TSV", RTAT, PPIMT, Hisar, 2012. 5. Sandeep Kumar, Kota Solomon Raju,

	<p>Deepak Kedia, “ Design of User Defined Instructions for Power PC 405 on Virtex-4 FPGA, ICIT, PDMCE, Bahadurgarh, Haryana, June 2009.</p> <p>6. Sandeep Kumar, Ashutosh Gupta and Deepak Kedia, “ Speed Optimization Technologies for 32-bit Binary Floating Point Multiplicers”, RTAC, JCDCE, Sirsa, Haryana, February, 2009.</p>
Organizing National Conference/ International Conference/ FDP/STTP	08
<ul style="list-style-type: none"> List of Conference/FDP/STTP committee 	<ol style="list-style-type: none"> National Conference on Emerging Trends in Electronic and Communication Engineering, PIET, Samalkha, 2013 Attended two day Training Programme on “SILVACO EDA AND TCAD TOOL (SETT)” organized by TIET, Patiala on April 8-9, 2019. Attended the Lecture Series on topic, “Partial Differential Equations and its Applications”, held at Thapar Institute of Engineering & Technology, Patiala on March, 29-30, 2019. Participated in One day National seminar on “Semiconductor Technology: Trends and Challenges”, sponsored by (TEQIP)-III at PEC, Chandigarh on 12th May, 2018. Participated in One week workshop on “Optimization using MATLAB through ICT” organized by NITTTR, Chandigarh at PIET, Samalkha in July, 2017. Participated in One week workshop on “Embedded System Practices through ICT” organized by NITTTR, Chandigarh at PIET, Samalkha in May, 2017. Participated in Conference titled “Contemporary Communication Technologies” organized by Deptt. of ECE, Guru Jambheshwar University of Science & Technology, Hisar on March 4th, 2008. Attended the National Level IMS (Indian Microelectronics Society) Conference 2006 held at Kurukshetra University, Kurukshetra from Feb 16-18th, 2006.
Social Contributions and Sports	
<ul style="list-style-type: none"> List of Social Contributions and Sports 	