Name: - Harish Saini **Subject Name: - COA**

Branch/Semester: - 5th Sem. **Subject Code:-CSE-307N**

Sr. No.	Lecture	Topics To Be Covered	Planned on	Covered On	Remarks
1	L 1	Introduction to Computer Systems, Organization and architecture	18.7.19		
2	L 2	Evolution and computer generations;	19. 7.19		
3	L 3	Fixed point representation of numbers	22. 7.19		
4	L 4	digital arithmetic algorithms for Addition and Subtraction	25. 7.19		
5	L 5	Multiplication using Booth's algorithm	26. 7.19		
6	L 6	Division using restoring and non restoring algorithms	29. 7.19		
7	L 7	Floating point representation with IEEE standards	1.8.19		
8	L 8	Floating Point arithmetic	2.8.19		
9	L 9	Floating Point arithmetic	5.8.19		
10	L 10	Instruction codes, stored program organization	8.8.19		
11	L 11	Computer registers and common bus system, computer instructions	9.8.19		
12	L 12	Computer registers and common bus system, computer instructions	12.8.19		
13	L 13	Timing and control, instruction cycle: Fetch and Decode	16.8.19		
14	L 14	Register reference instructions; Memory reference instructions.	19.8.19		
15	L 15	Input, output and Interrupt: configuration, instructions	22.8.19		
16	L 16	Program interrupt, Interrupt cycle	23.8.19		
17	L 17	Micro programmed Control organization, address sequencing	26.8.19		
18	L 18	Micro instruction format	29.8.19		
19	L 19	microprogram sequencer	30.8.19		
20	L 20	Unit-III: Central Processing Unit: General register organization	2.9.19		

21	L 21	stack organization, instruction formats	5.9.19		
22	L 22	stack organization, instruction formats	6.9.19		
23	L 23	Numerical on Instruction Formats	9.9.19		
24	L 24	Addressing modes	12.9.19		
25	L 25	Addressing modes	13.9.19		
26	L26	Numerical on Addressing Modes	16.9.19		
27	L 27	Data transfer and manipulation, Program control.	19.9.19		
28	L 28	CISC and RISC: features and comparison	26.9.19		
29	L 29	Pipeline and vector Processing, Parallel Processing	27.9.19		
30	L 30	Pipelining, Instruction Pipeline	30.9.19		
31	L 31	Numerical on Pipelining	3.10.19		
32	L 32	Basics of vector processing and Array Processors. I/O interface. I/O Bus and interface modules	4.10.19		
33	L 33	I/O versus Memory Bus.Asynchronous data transfer:	7.10.19		
34	L34	Strobe control, Handshaking	10.10.19		
35	L 35	Asynchronous serial transfer.	11.10.19		
36	L 36	Modes of Transfer: Programmed I/O, Interrupt driven I/O	14.10.19		
37	L 37	Priority interrupt; Daisy chaining	17.10.19		
38	L 38	Parallel Priority interrupts.	24.10.19		
39	L 39	Direct memory Access, DMA controller and transfer.	25.10.19		
40	L 40	Input output Processor, CPU-IOP communication, I/O channel.	31.10.19		
41	L 41	Input output Processor, CPU-IOP communication, I/O channel.	4.11.19		

42	L 42	**Content Beyond Syllabus- Memory Organization- Memory Hierarchy**	7.11.19		
43	L 43	**Cache Organization**	8.11.19		
44	L 44	**Mapping Techniques- Direct Mapping**	11.11.19		
45	L 45	**Associative Mapping and Set Associative Mapping**	14.11.19		
46	L 46	**Virtual Memory**	15.11.19		
47	L 47	Revision	18.11.19		