PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY

Department Of Electronics & Communication Engineering

LESSON PLAN

Subject Name: - Computer Organization and Architecture **Subject Code: - EC-305A**
Year: - 3rd **Semester:-5th**

Lecture No.	UNIT NO.	Topics	References
L 1	**UNIT 1**:	**Digital Logic Circuits:** Basic Logic Functions, Synthesis of Logic Functions Using AND, OR, and NOT Gates	M. Moris Mano, "C
L 2		Minimization of Logic Expression	M. Moris Mano, "C
L 3		Synthesis with NAND and NOR Gates	M. Moris Mano, "C
L 4		Flip-Flops, Registers and Shift Registers	M. Moris Mano, "C
L 5		Counters, Decoders, Multiplexers	M. Moris Mano, "C
L 6		Programmable Logic Devices (PLDs)	M. Moris Mano, "C
L 7		**Basic Structure of Computers:** Functional units, Basic operational concepts, Bus structures	M. Moris Mano, "C
L 8		Software,Performance,multiprocessors and multicomputers	M. Moris Mano, "C
L 9		**Content beyond the syllabus**	M. Moris Mano, "C

L 10		Encoders	M. Moris Mano, "C
L 11	**UNIT 2**:	DeMultiplexers	M. Moris Mano, "C
L 12		Programmable Logic Arrays (PLAs)	M. Moris Mano, "C
L 13		Programmable Logic Arrays (PLAs)	M. Moris Mano, "C
L 14		**Data Representation:** Data types, Complements	M. Moris Mano, "C
L 15		Other binary codes, Error Detection codes	M. Moris Mano, "C
L16		**Register and Micro operations:** Register Transfer language,	M. Moris Mano, "C
L 17		Arithmetic Micro operations, logic micro operations	M. Moris Mano, "C
L 18		Shift micro operations, Arithmetic logic shift unit	M. Moris Mano, "C
L 19		**Content beyond the syllabus**	M. Moris Mano, "C
L 20	**UNIT 3**:	Gray code, Excess-3 code	M. Moris Mano, "C
L 21		Circuits for all micro operations	M. Moris Mano, "C
L 22		Computer Instructions, Instruction Cycle, Memory Reference	M. Moris Mano, "C
L 23		Instructions	M. Moris Mano, "C
L 24		Hardwired Control, Micro Programmed Control	M. Moris Mano, "C
L25		Register Transfer Bus and memory transfers	M. Moris Mano, "C
L 26		Register organization, Stack organization, Instruction formats	M. Moris Mano, "C

L 27	**UNIT 4**:	Addressing modes, Data Transfer and manipulations, RISC,	M. Moris Mano, "C
L 28		CISC	M. Moris Mano, "C
L 29		**Computer Arithmetic:** Addition, subtraction, multiplication	M. Moris Mano, "C
L 30		division operations, Floating point Arithmetic operations	M. Moris Mano, "C
L 31		**Content beyond the syllabus**	M. Moris Mano, "C
L 32		Types of instruction formats	M. Moris Mano, "C
L 33		Control unit	M. Moris Mano, "C
L 34		Control unit	M. Moris Mano, "C
L 35		**Input-Output Organization:** Peripheral Devices, Input-	M. Moris Mano, "C
L 36		Output Interface	M. Moris Mano, "C
L 37		Asynchronous data transfer, Modes of Transfer	M. Moris Mano, "C
L 38		Priority Interrupt, Direct memory Access	M. Moris Mano, "C
L39		RAM,ROM secondary memory	M. Moris Mano, "C

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Text Books:

1. M. Moris Mano, "Computer Systems Architecture", 4th Edition, Pearson/PHI,ISBN 10:01

2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, “Computer Organization”, 5th Edition,McGraw Hill.

Reference Book:

1. John L. Hennessy and David A. Patterson, “Computer Architecture a quantitativeapproach”, 4th Edition Elsevier, ISBN:10:0123704901
2. William Stallings, “Computer Organization and Architecture”, 6th Edition, Pearson/PHI,ISBN:10:0-13-609704-9
3. Donald e Givone, “Digital Principles and Design”, TMH. A.Anandkumar, “Fundamentals of digital circuits”, 4th edition, PHI