PANIPAT INSTITUTE OF ENGINEERING AND TECHNOLOGY
PANIPAT
Department of Information Technology
LESSON PLAN

Name: - Ms. Payal **Subject Name: - Computer Architecture & Organization**
Branch/Semester: - 5th SEM **Subject Code: - PC-IT-305A**

Sr. No.	Lecture No.	Topics To Be Covered	Covered On	Remarks
1.	L 1	UNIT-1: Introduction of COA and its difference		
2.	L 2	Von-Neumann Model		
3.	L 3	Store program control concept		
4.	L 4	Flynn's classification of computers(SISD)		
5.	L 5	Introduction of MISD,MIMD		
6.	L 6	Multilevel viewpoint of a machine		
7.	L 7	Digital logic: AND ,OR, NOT		
8.	L 8	Digital logic: EX-OR,EXNOR etc.		
9.	L 9	Introduction to Micro architecture		
10.	L 10	Explain ISA with its functionality		
11.	L 11	Introduction to operating systems		
12.	L 12	Languages: High level language, low level, assembly language		
13.	L 13	CPU and its instruction cycle		
14.	L 14	secondary memory units& I/O		
15.	L 15	caches, main memory		
16.	L 16	Instruction Codes		
17.	L 17	Computer registers		
18.	L 18	Computer Instructions		
19.	L 19	Timing and Control		
20.	L 20	Instruction Cycle		
21.	L 21	Type of Instructions: Memory reference instructions, Register reference instructions.		
22.	L 22	Type of Instructions : Input output instructions Design of accumulator logic		
23.	L 23	UNIT 2: Register Transfer and Micro operations		
24.	L 24	Register Transfer Language (RTL), register transfer		

25.	**L 25**	Bus and Memory Transfers		
26.	**L 26**	Arithmetic Micro operations		
27.	**L 27**	Logic Micro operations		
28.	**L 28**	Shift Micro operations		
29.	**L 29**	Arithmetic Logic Shift Unit		
30.	**L 30**	Micro programmed Control: Control memory		
31.	**L 31**	address sequencing, micro program sequencer		
32.	**L 32**	CPU Architecture types (accumulator, register, stack, memory/register), Program Control.		
33.	**L 33**	Instruction formats, Addressing Modes, Data Transfer and Manipulation		
34.	**L 34**	Program Interrupt, RISC, CISC		
35.	**L 35**	Memory hierarchy, Main memory (Semiconductor RAM& ROM organization, memory expansion, Static & dynamic memory types);		
36.	**L 36**	Cache memory (Associative& direct mapped cache organizations.		
37.	**L 37**	Auxiliary Memory, Associative Memory		
38.	**L 38**	Cache memory, Virtual Memory		
39.	**L39**	Direct Memory Access (DMA), Input-Output Processor (IOP).		
40.	**L 40**	Revision/Previous Years university question papers		

(COURSE INCHARGE)