PANIPAT INSTITUTE OF ENGINEERING AND TECHNOLOGY
PANIPAT
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

LESSON PLAN

Name: -Shikha Singhal **Subject Name:-Digital Electronics**

Branch/Semester: -3rd Sem **Subject Code:-ES-207**

Sr. No.	Lecture No.	Topics To Be Covered	Planned on	Covered On	Remarks
1.	L1	Unit-1: Introduction of Digital Electronics	16/7/19		
2.	L2	Some basics of Number System	17/7/19		
3.	L3	Logic Gates: AND, OR, NOT, NAND, NOR	19/7/19		
4.	L4	Exclusive-OR and Exclusive NOR gates	22/7/19		
5.	L5	Implementation of Logic Functions using gates	23/7/19		
6.	L6	NAND- NOR Implementation	24/7/19		
7.	L7	Gate Multilevel Implementation	26/7/19		
8.	L8	Boolean Postulates	27/7/19		
9.	L9	Laws of Boolean algebra	29/7/19		
10.	L10	De-Morgan's Theorem,	30/7/19		
11.	L11	Principle of duality and Boolean Expression Simplification	31/7/19		
12.	L12	Minterms, Maxterms, SOP, POS	2/8/19		
13.	L13	K-map techniques	5/8/19		
14.	L14	K Map minimization problems	6/8/19		
15.	L15	Quine -Mccluskey method on SOP question	7/8/19		
16.	L16	Q M method on POS, don't care condition	9/8/19		
17.	L17	Q M method questions	12/8/19		
18.	L18	TTL with NAND gate	13/8/19		
19.	L19	CMOS with NAND & its characteristics	14/8/19		
20.	L20	**Unit-2**: Half Adder & Full Adder	16/8/19		
21.	L21	Half Subtractor & Full Subtractor	19/8/19		
22.	L22	Parallel Binary Adder, Parallel Binary Subtractor	20/8/19		
23.	L23	Fast & Carry Look Ahead Adder,	21/8/19		
24.	L24	Serial Adder/Subtractor	23/8/19		

25.	L25	BCD adder/Subtractor	26/8/19		
26.	L26	Decoder,	27/8/19		
27.	L27	Encoder	28/8/19		
28.	L28	Multiplexer Description	30/8/19		
29.	L29	Demultiplexer Description	2/9/19		
30.	L30	Demultiplexer	3/9/19		
31.	L31	Parity Generator and checker	4/9/19		
32.	L32	Test	6/9/19		
33.	L33	**Unit 3**:Flip flop and latch concept	9/9/19		
34.	L34	Edge Triggering, Level Triggering,	10/9/19		
35.	L35	Realization of Flip-Flop using other flip-flops.	11/9/19		
36.	L36	Serial adder, subtractor,	13/9/19		
37.	L37	Asynchronous Ripple or serial counter	16/9/19		
38.	L38	UP/Down Counter	17/9/19		
39.	L39	Synchronous Counter	18/9/19		
40.	L40	Synchronous up/down counter	25/9/19		
41.	L41	Programmable Counters,	27/9/19		
42.	L42	Design of Synchronous Counter	30/9/19		
43.	L43	State diagram description	1/10/19		
44.	L44	State table, state minimization	4/10/19		
45.	L45	State assignment	9/10/19		
46.	L46	Excitation table	11/10/19		
47.	L47	Maps implementation	14/10/19		
48.	L48	Modulo-n counter ,shift registers, Universal shift register	15/10/19		
49.	L49	555 timer, shift registers introduction	16/10/19		
50.	L50	Types of shift registers, Shift register counter	18/10/19		
51.	L51	Ring counter, Sequence generator	25/10/19		
52.	L52	**Unit-4**: Classification of Memories: RAM, ROM, PROM, EPROM, EEPROM, EAPROM	4/11/19		
53.	L53	RAM organization, Write operation, Read operation, Memory cycle, Timing waveforms	5/11/19		
54.	L54	A/D Convertors	6/11/19		
55.	L55	D/A Convertors	8/11/19		
56.	L56	Memory decoding, memory	11/11/19		

		expansion, Static and bipolar RAM cells MOSFET RAM cells, Dynamic RAM Cells			
57.	L57	Programmable Logic devices (PLA), PAL.	13/11/19		
58.	L58	PLA using ROM	15/11/19		
59.	L59	Revision	18/11/19		